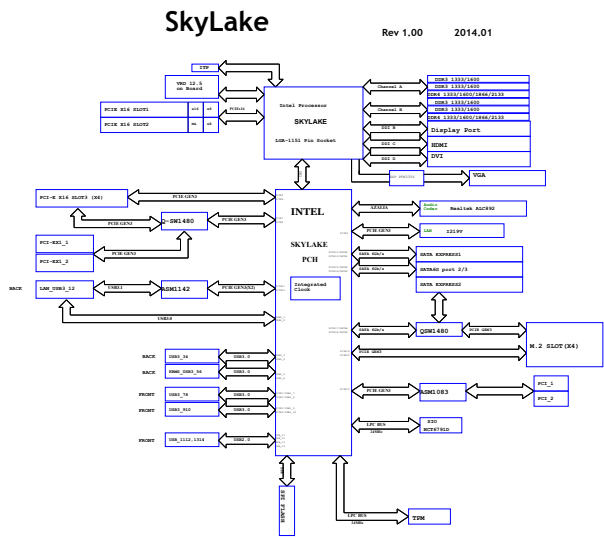
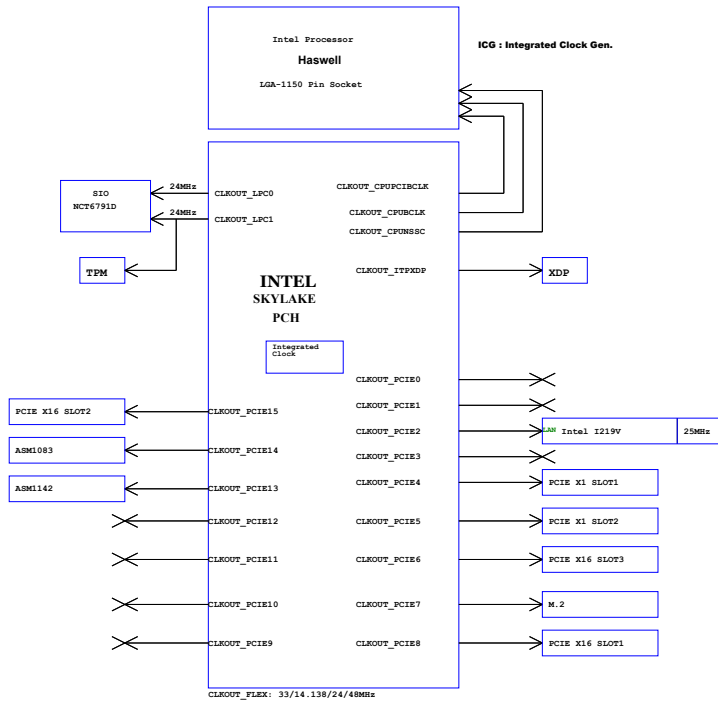
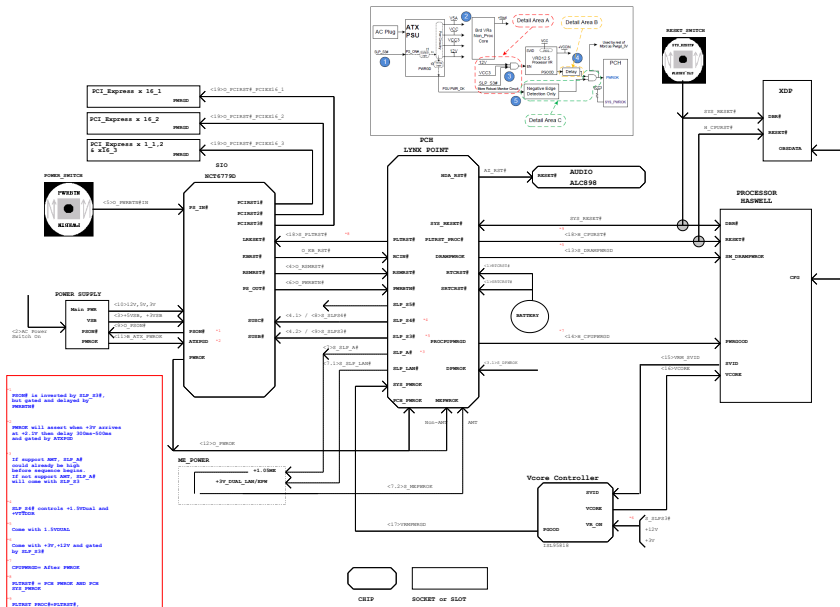
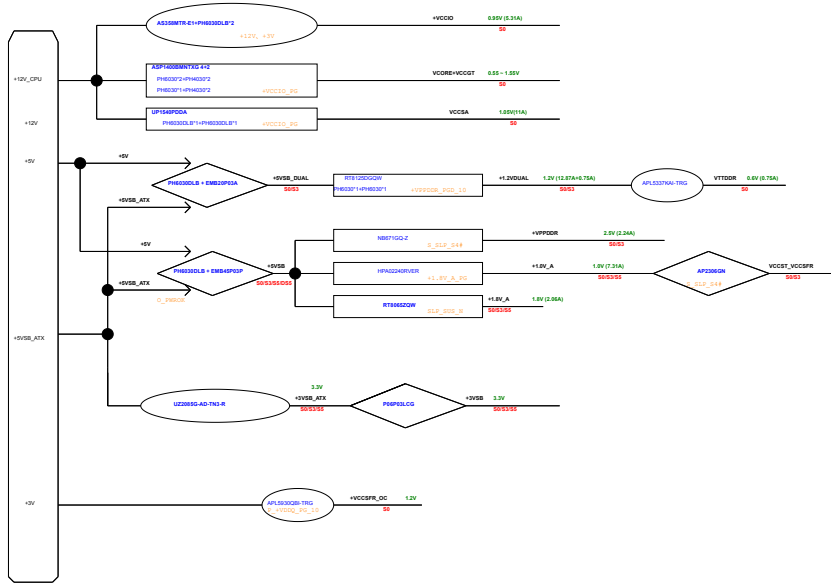


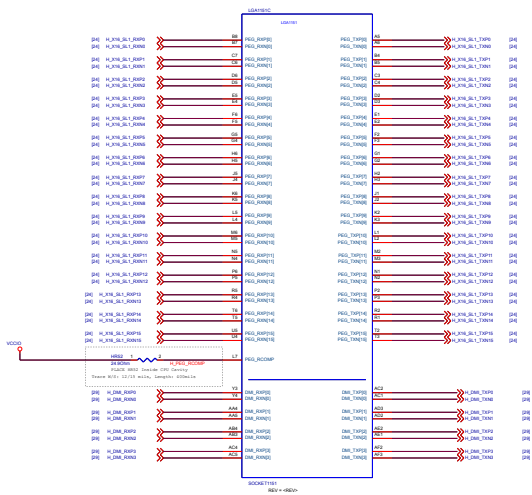
H110M-D D3 1.01

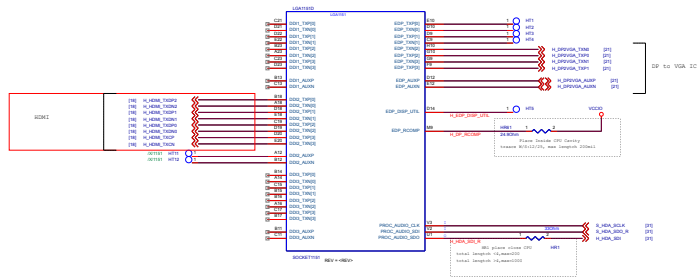


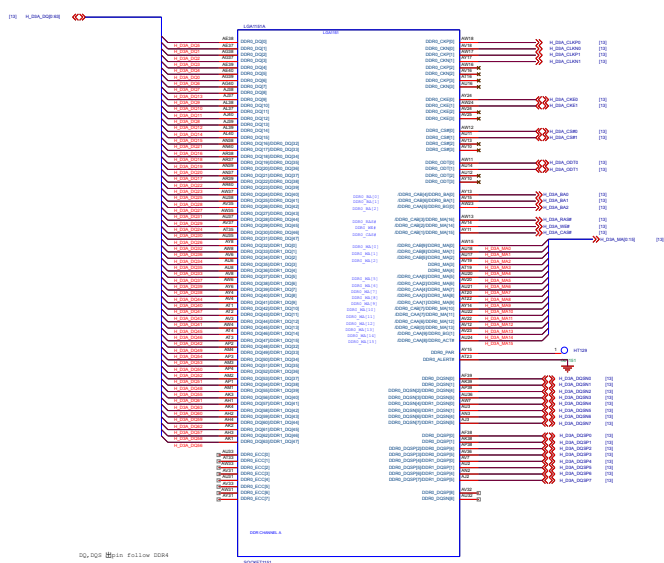


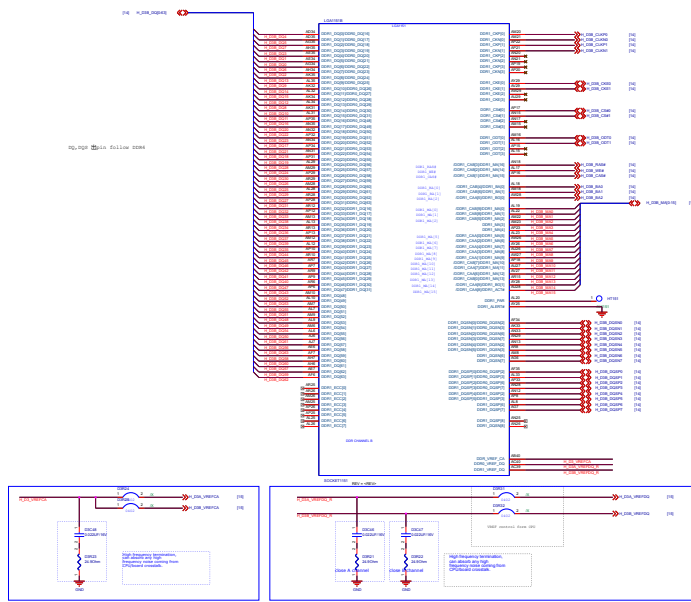


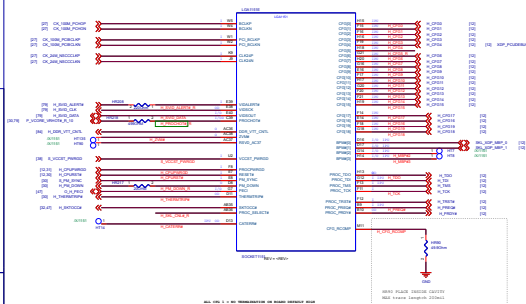












MSB 000 1 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 2 = INTERNAL WRECK LINE ON BOARD

MSB 000 3 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 4 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 5 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 6 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 7 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 8 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 9 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 10 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 11 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 12 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 13 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 14 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 15 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 16 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 17 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 18 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 19 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 20 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 21 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 22 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 23 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 24 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 25 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 26 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 27 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 28 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 29 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 30 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

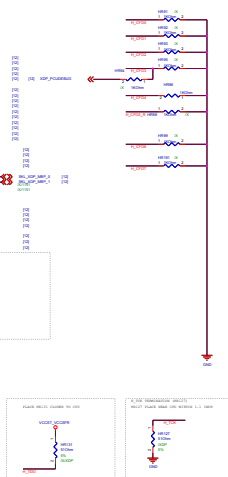
MSB 000 31 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

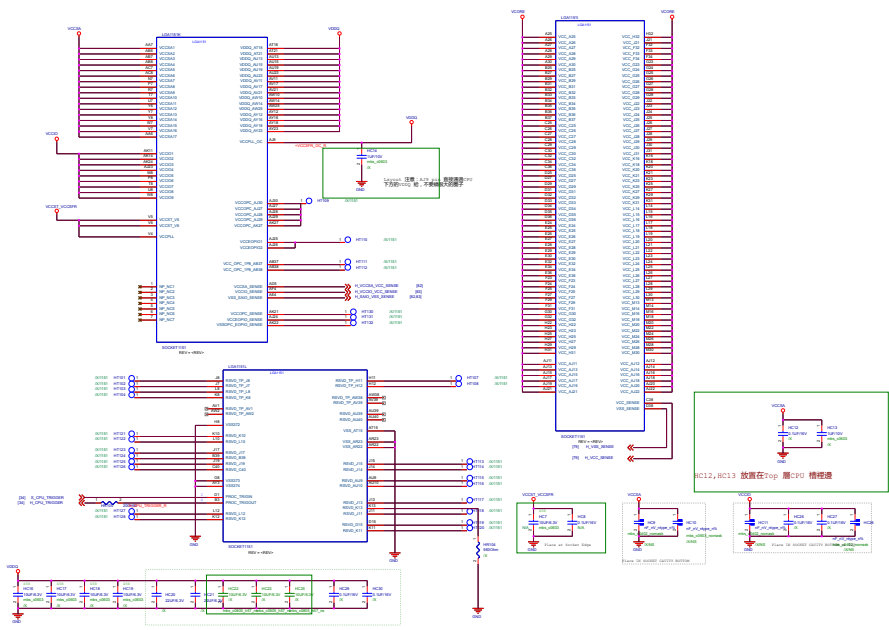
MSB 000 32 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

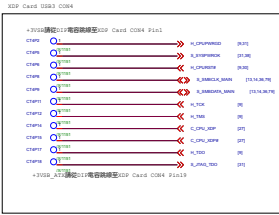
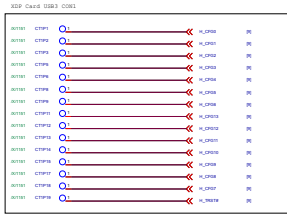
MSB 000 33 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 34 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

MSB 000 35 = 00 TRANSMISSION ON BOARD ORIENTAL AIR

[illegible]

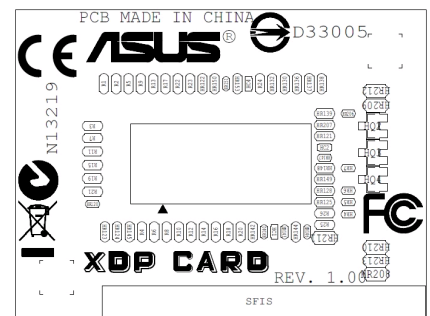


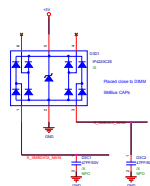
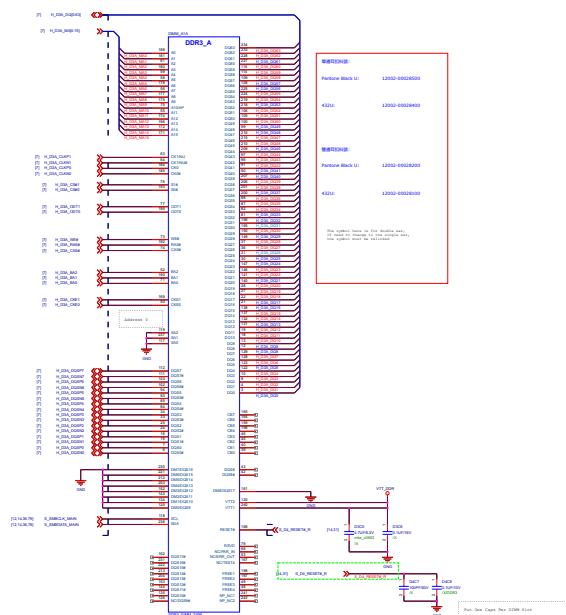


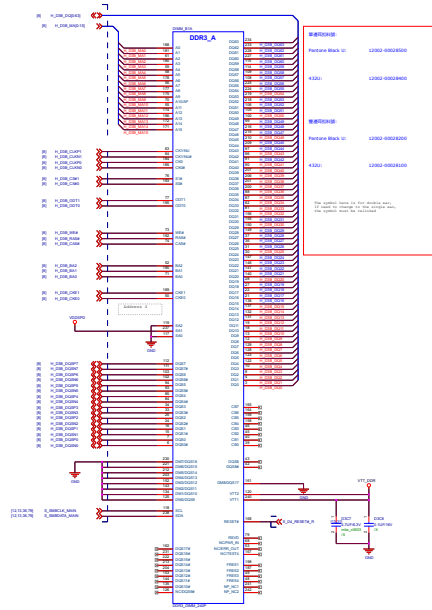
Binding Rule:
C1P15~C1P0: 16 pins connected to H_PIO15~H_PIO0

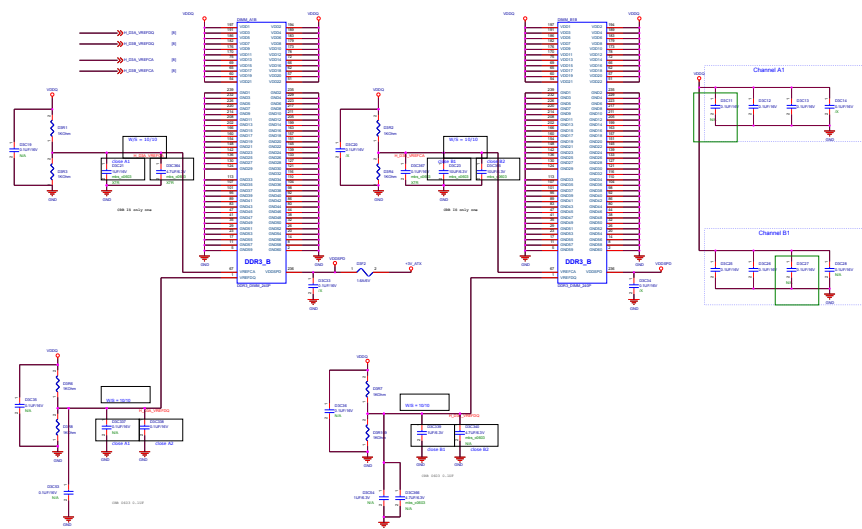
Placement Rule:
此圖為XDP卡針腳與主機板針腳之對應關係。
Layout時請依照此圖之針腳位置進行佈局。
若有需求時請以C1P15~C1P0之針腳位置為準。
但此圖僅供參考，H_PIO15~H_PIO0之針腳位置請以主機板為準。

Power Rule:
+1.0V: 16 pins connected to H_PIO15~H_PIO0
+3.0V: 16 pins connected to H_PIO15~H_PIO0
+5.0V: 16 pins connected to H_PIO15~H_PIO0
+12V: 16 pins connected to H_PIO15~H_PIO0
GND: 16 pins connected to H_PIO15~H_PIO0

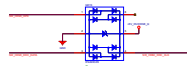
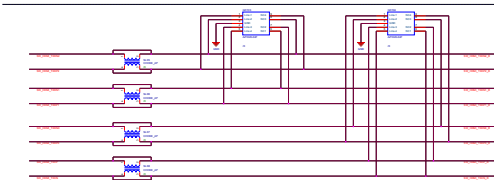
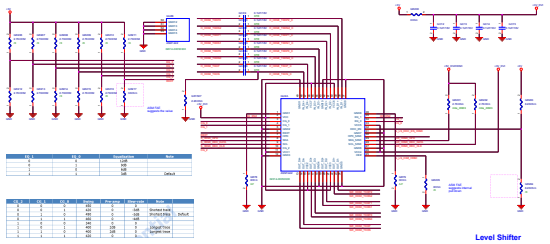




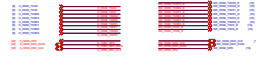


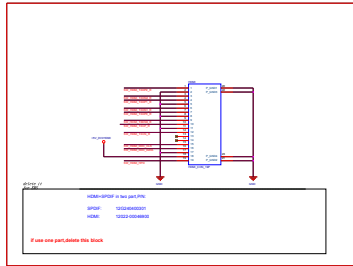
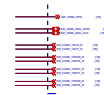


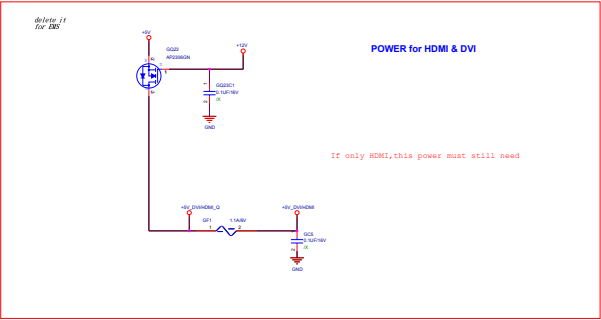
delete this page for HDMI-DVI copy



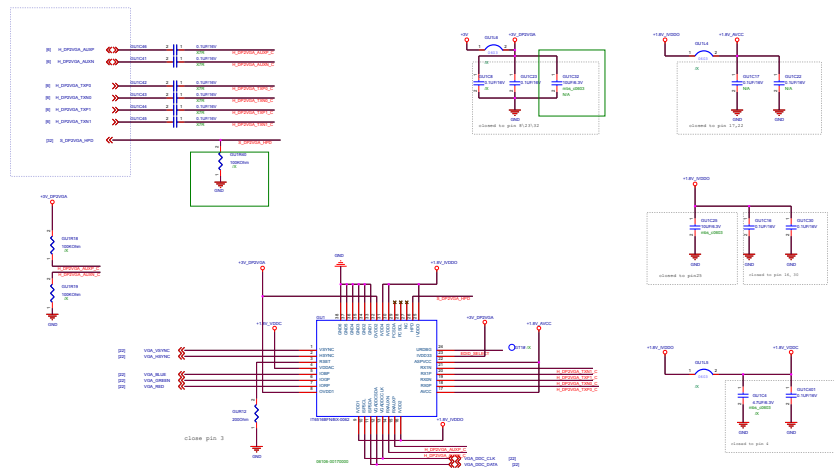
ESD

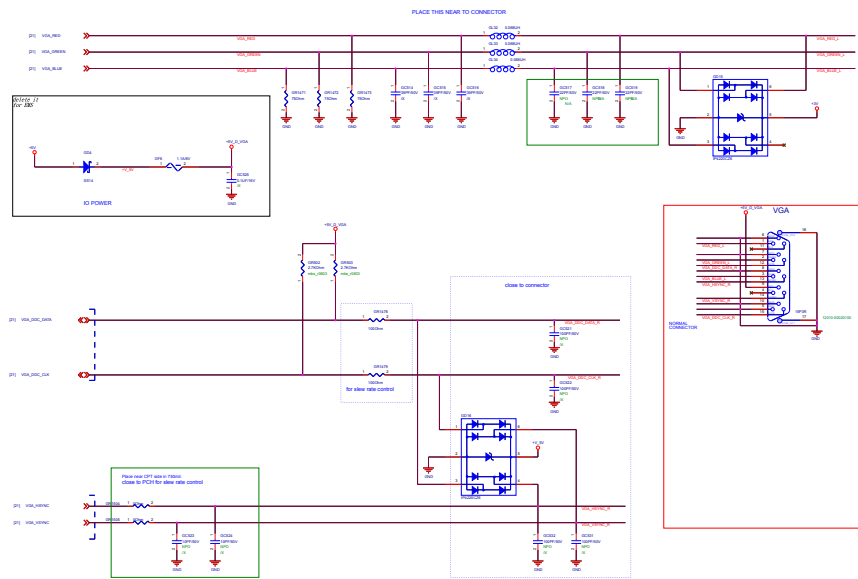


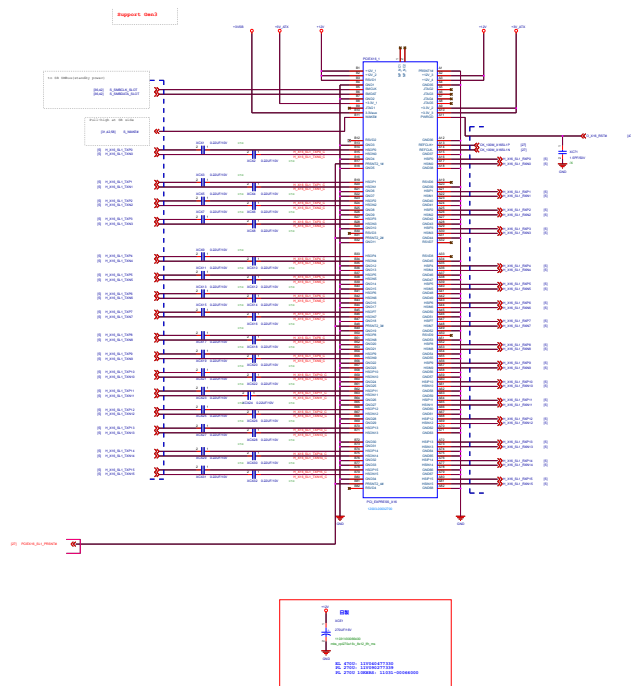


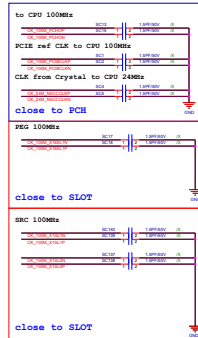
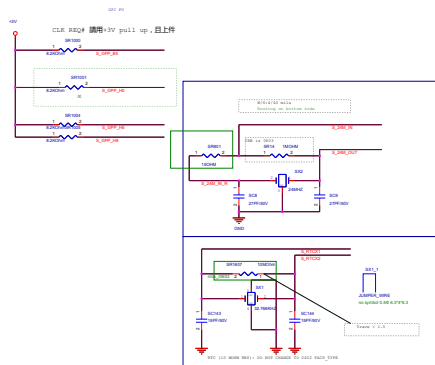
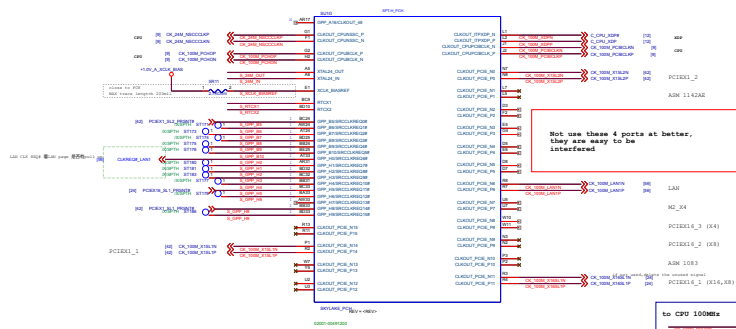


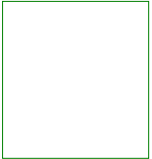
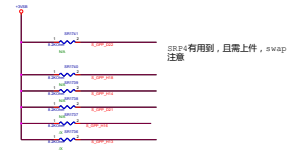
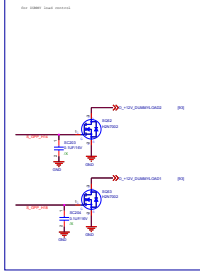
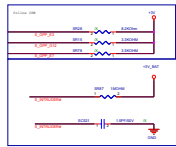
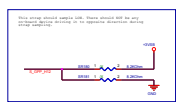
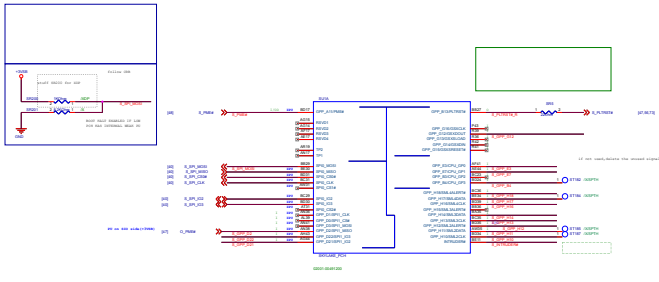
Passive/Active Devices					
Max Capacitance (Backdrive 1 Protection)	Schottky Diode	NA	pF	10	10
Resistor Value (+/- 5%)	R1R2	NA	Ω	680	NA
ESD Protection	ESD	NA	NA	Optional	Optional
Max nFET Body/Cout	NA	NA	Ω/pF	30nm/10pF	NA

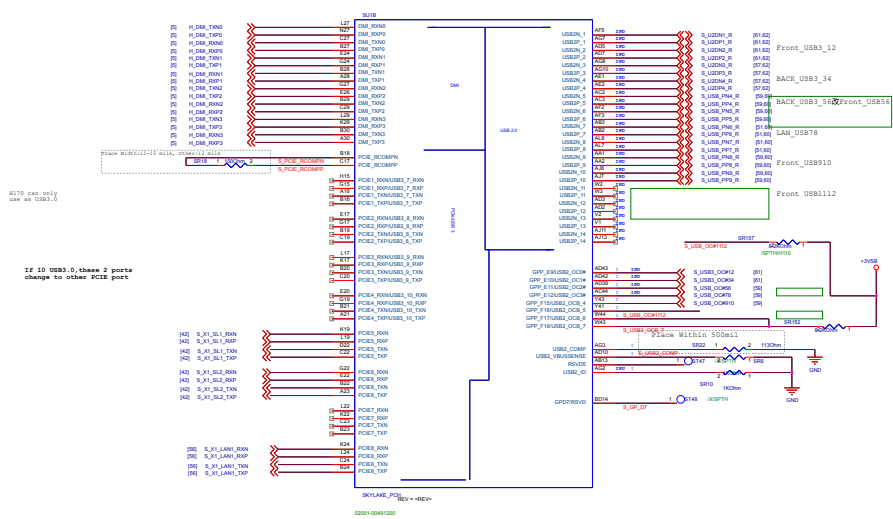


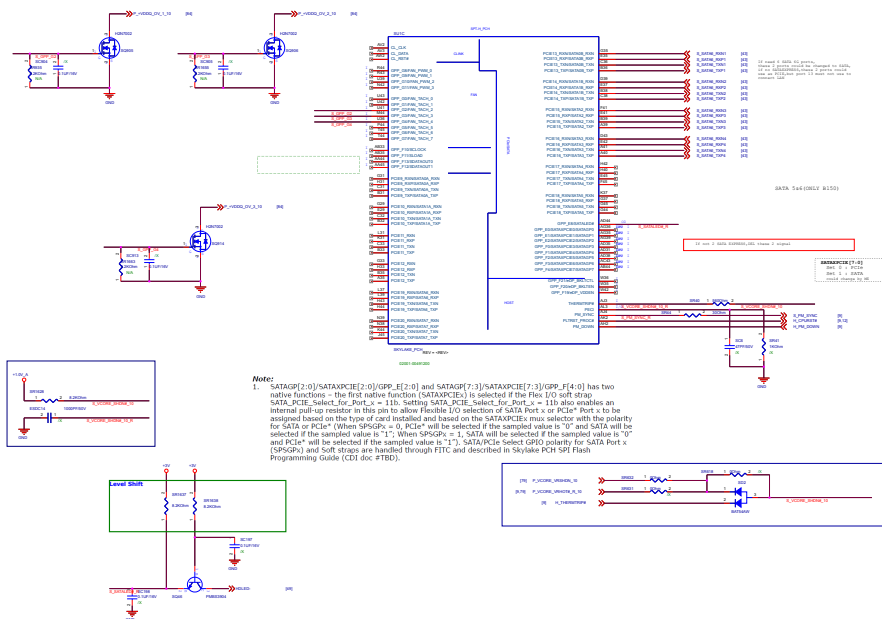


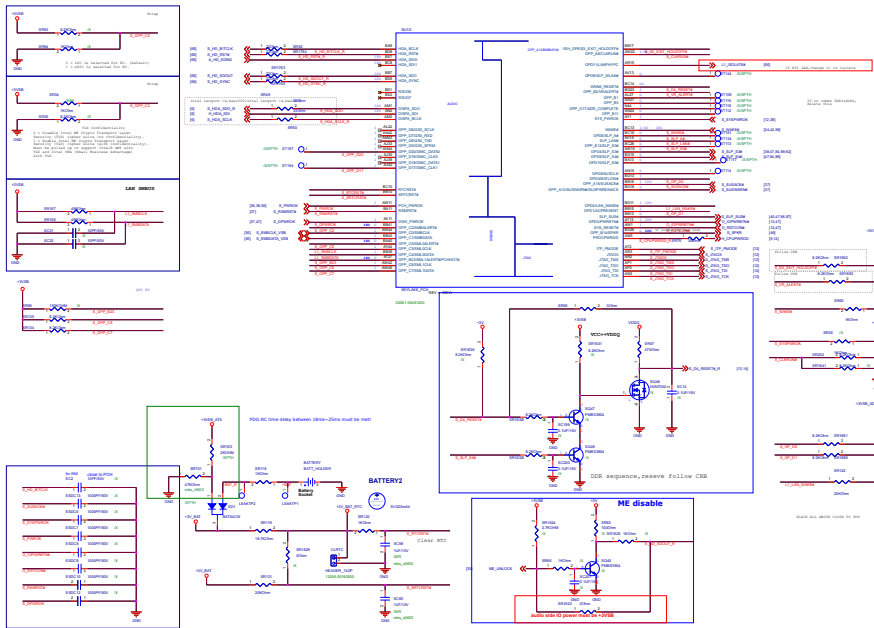


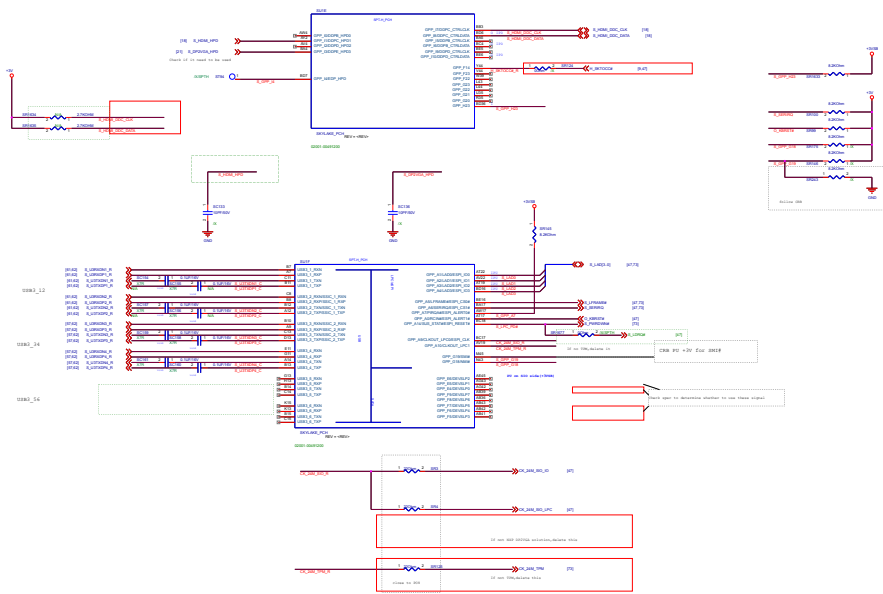


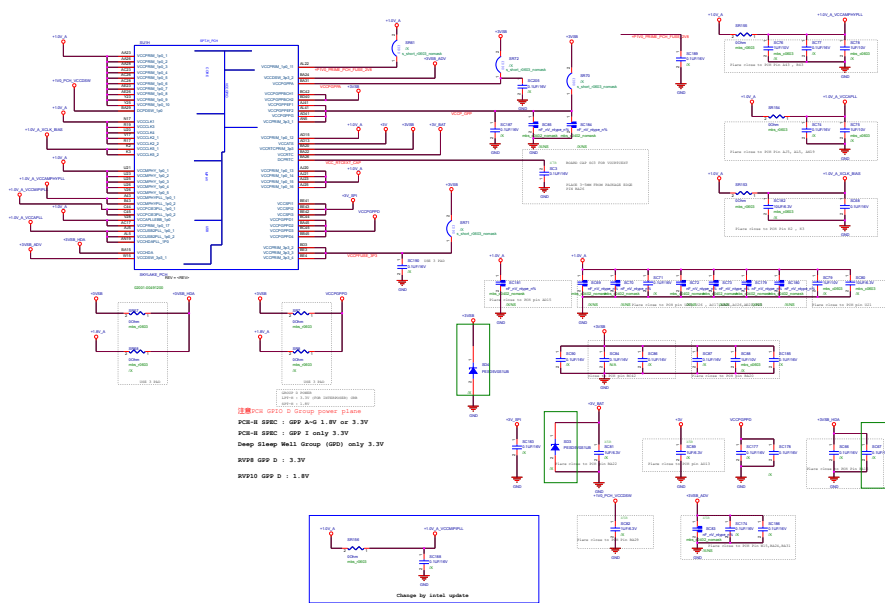


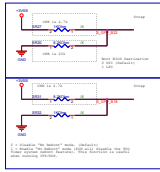




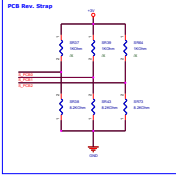
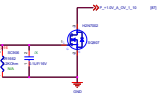
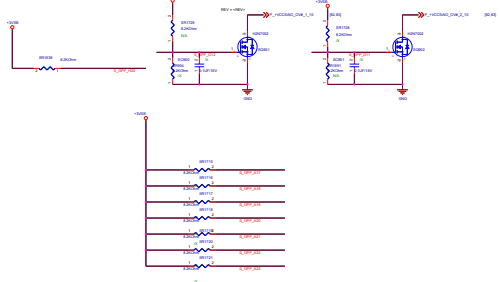


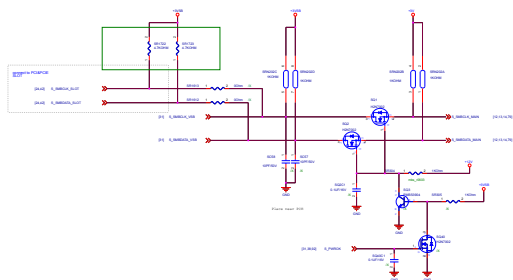




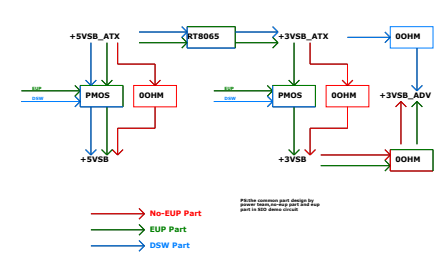


If the output here is not correct, the GND must be the pin's high for 700k kbps





POWER FLOW

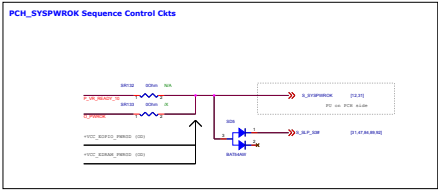
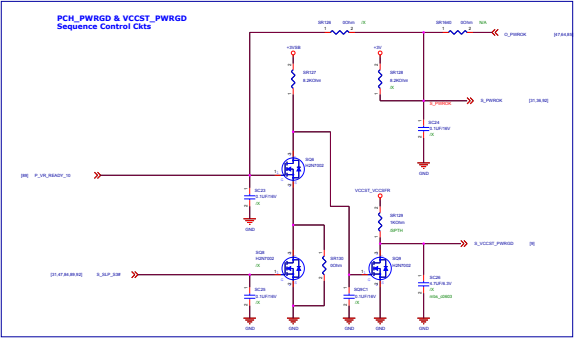


NOT SUPPORT DSW

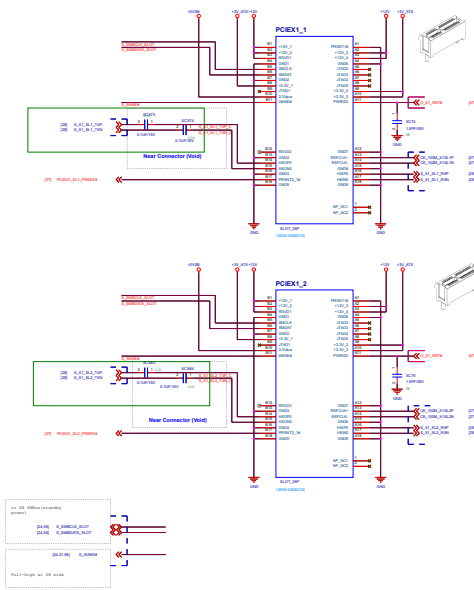


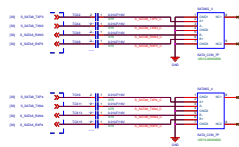
SUPPORT DSW





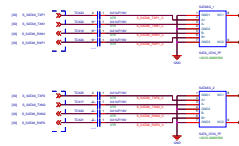
1. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
2. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
3. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
4. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
5. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
6. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
7. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
8. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
9. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.
10. PCH will have a minimum of a 100ms delay from the PWRGD to the start of the PCH_SYSPWRON signal.



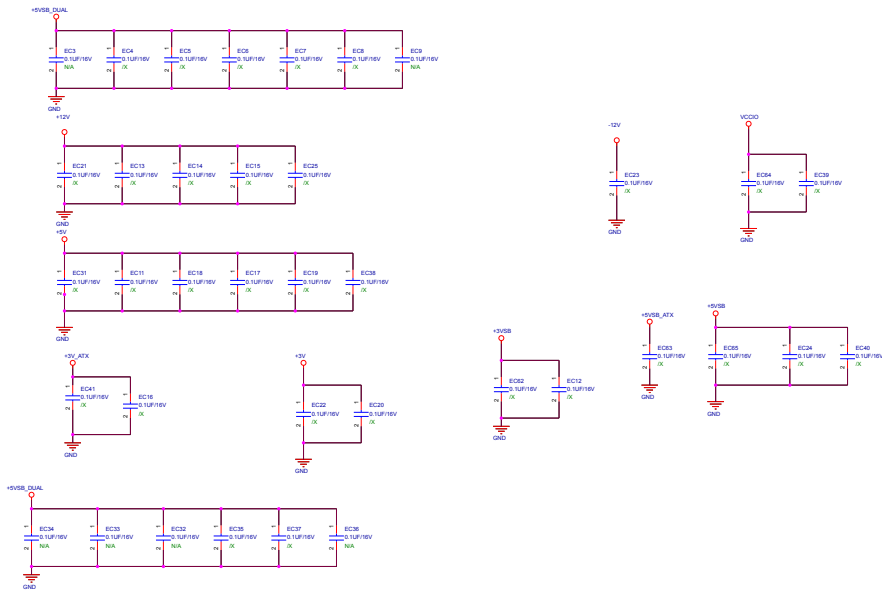


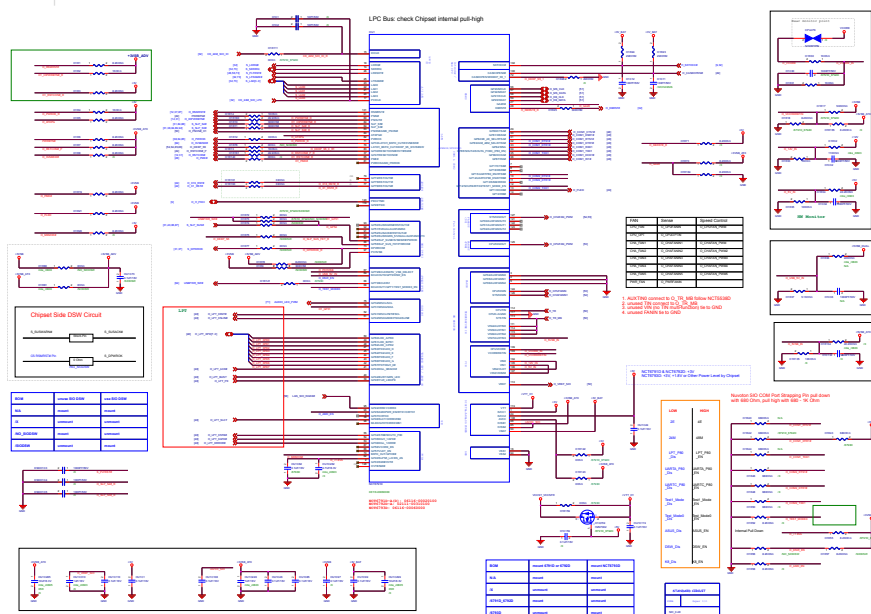
180度connector

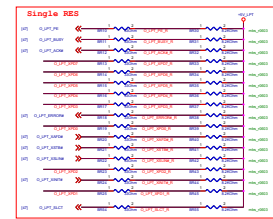
180° phase shifter



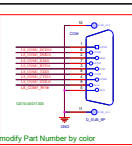
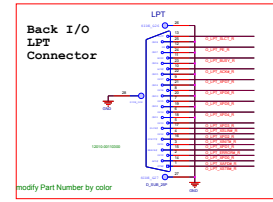
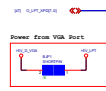
180度connector



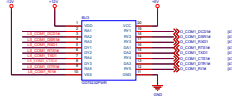
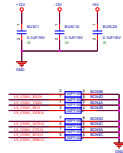
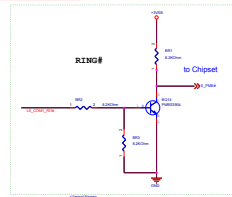


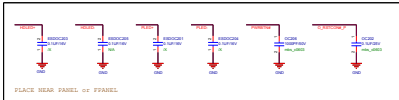


LPT PORT

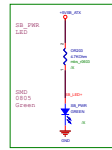
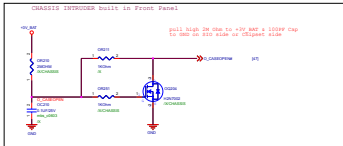
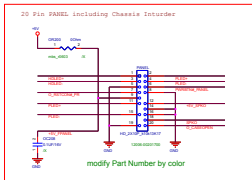
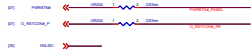


COM PORT



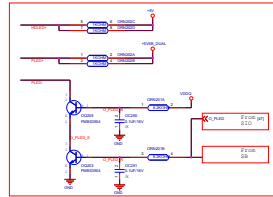


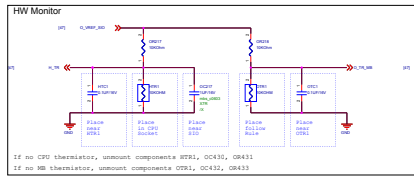
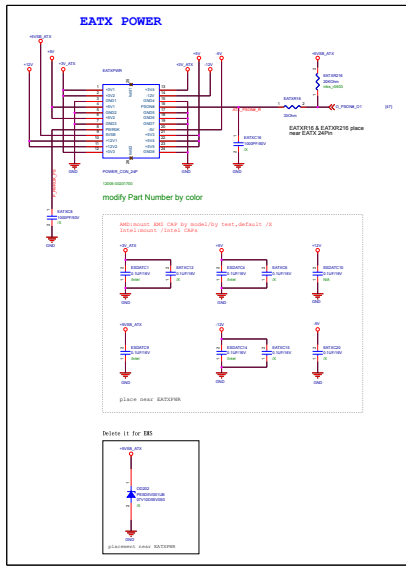
If change to single resistor, use
75 Ohm (0.0175/0.010)

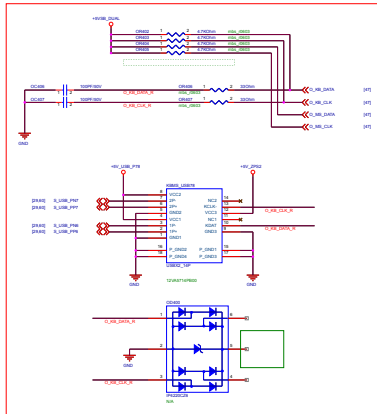


1. 25 Pin PANEL, including Chassis Interlock
2. 25 Pin PANEL, including Chassis Interlock
3. 25 Pin PANEL, including Chassis Interlock
4. 25 Pin PANEL, including Chassis Interlock
5. 25 Pin PANEL, including Chassis Interlock

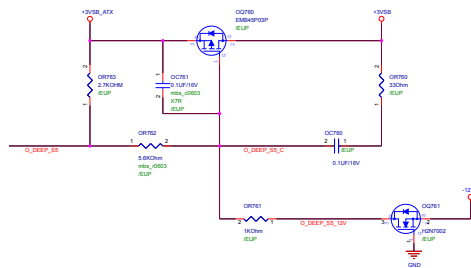
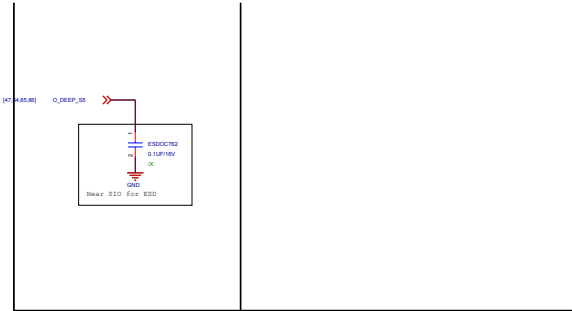
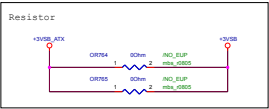
Power LED power source use +5VSB_DUAL

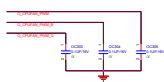




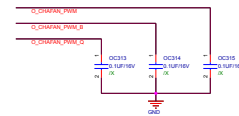
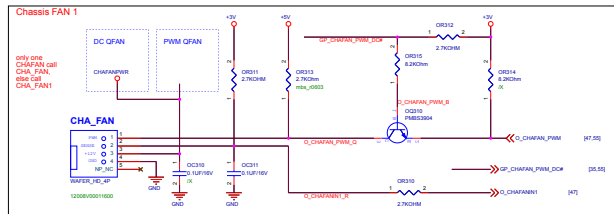


ERP Circuit

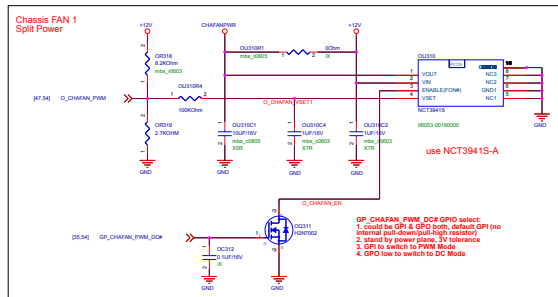


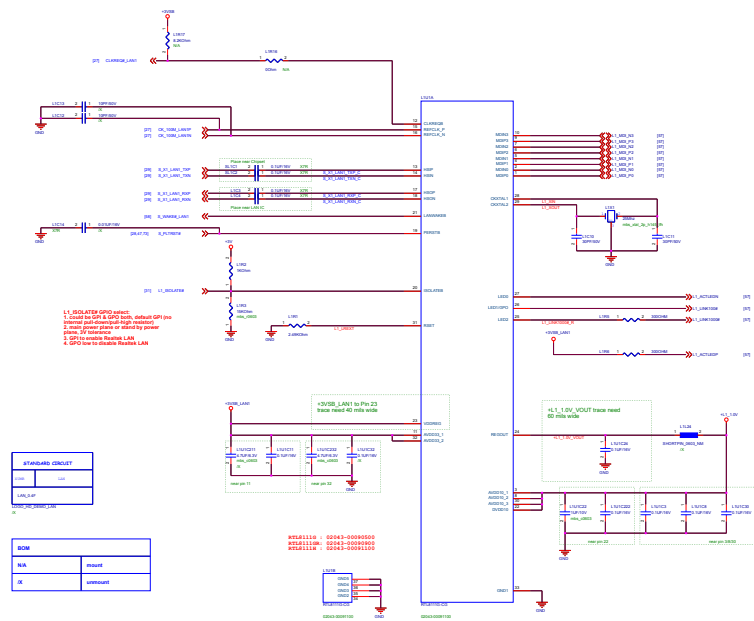


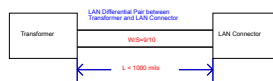
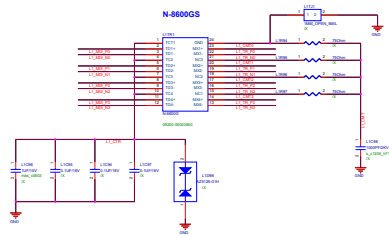
4 Pin PWM Mode & DC Mode



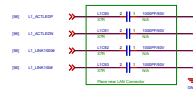
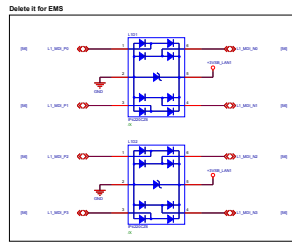
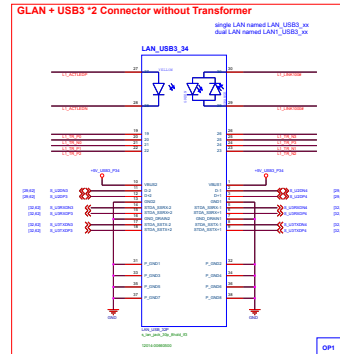
PWM Mode & DC Mode Power Solution







LAN Connector without Transformer



LAN1 POWER

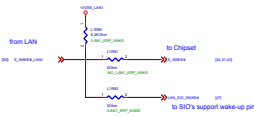
1. LAN IC power change to +3VSB_ATX (remove short pin L1R88, add resistor L1R88 & L1R89)

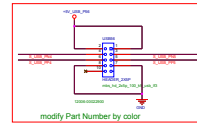
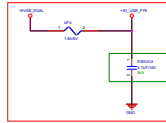
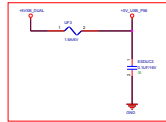
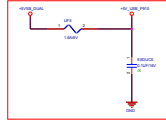
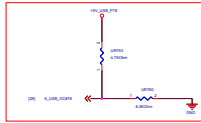
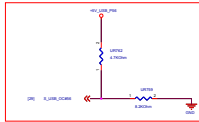


for PCIE LAN1

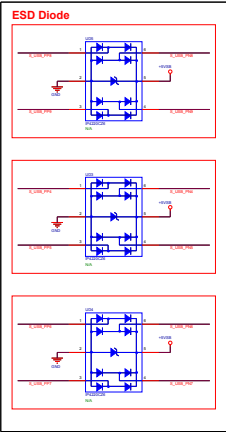
5. for Intel PCIE LAN, L1_DEV_OFF# choose +3VSB_ATX power plane GPIO

6. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN IC Page

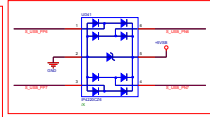
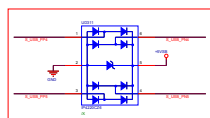
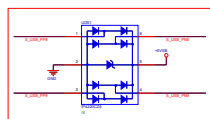
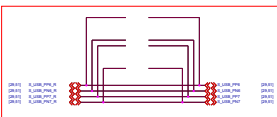
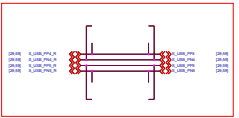
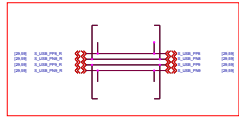




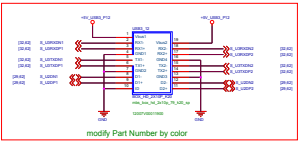
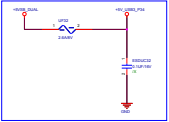
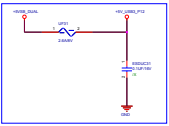
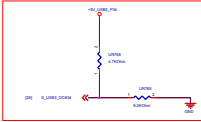
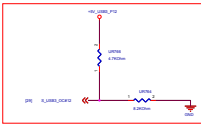
Refer to the DB



Reserve Location (RES A)

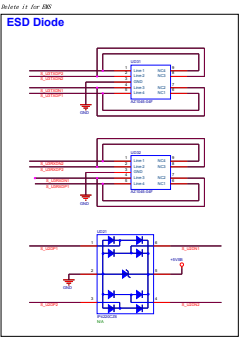


OC# circuit for Intel

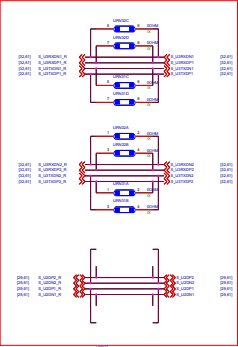


modify Part Number by color

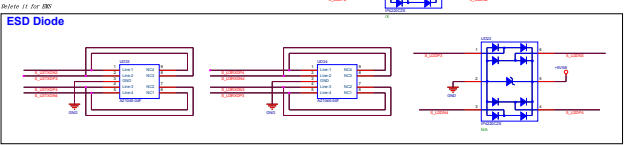
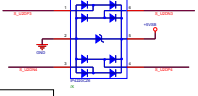
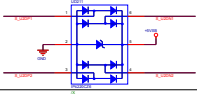
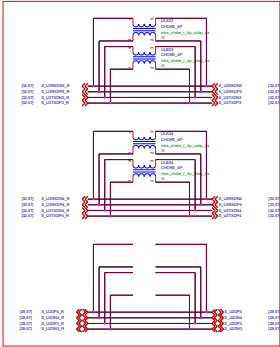
Port 12



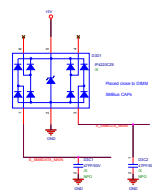
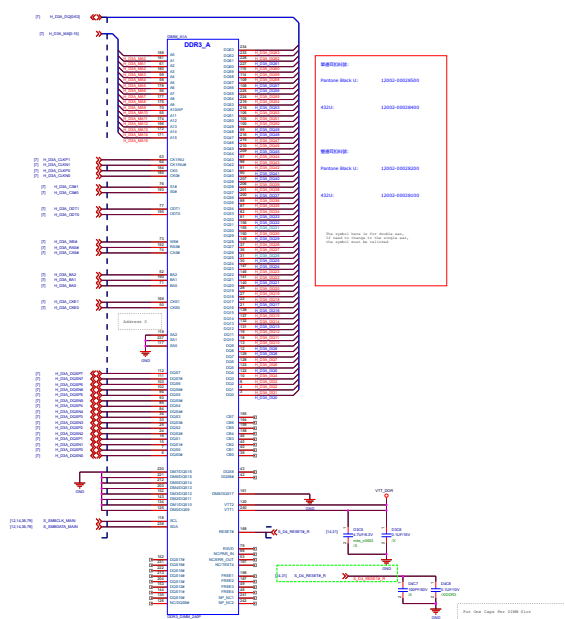
Reserve Location (RES A)

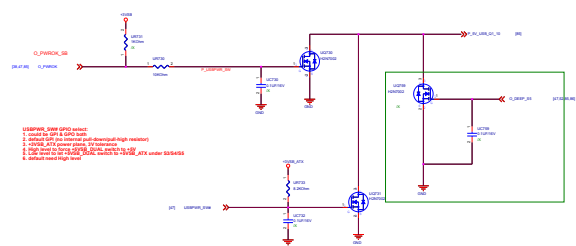


Reserve Location (Single RES)

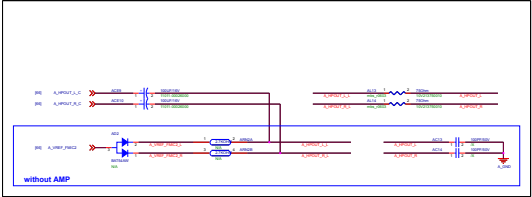


Port 34





for ALC887-VD2/ALC892/ALC1150



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Q5P, Q5N
M9, M10
Q6P, Q6N
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10uF

10uF

without AMP/De-POP

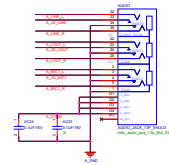
for Games Project, Line in use 10uF DIP CAP ACE12

Normal

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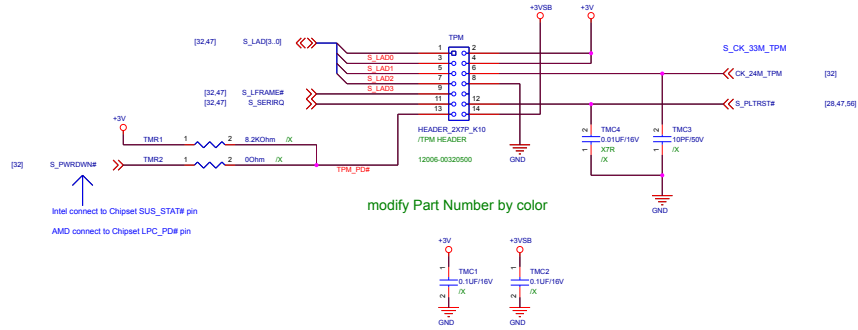
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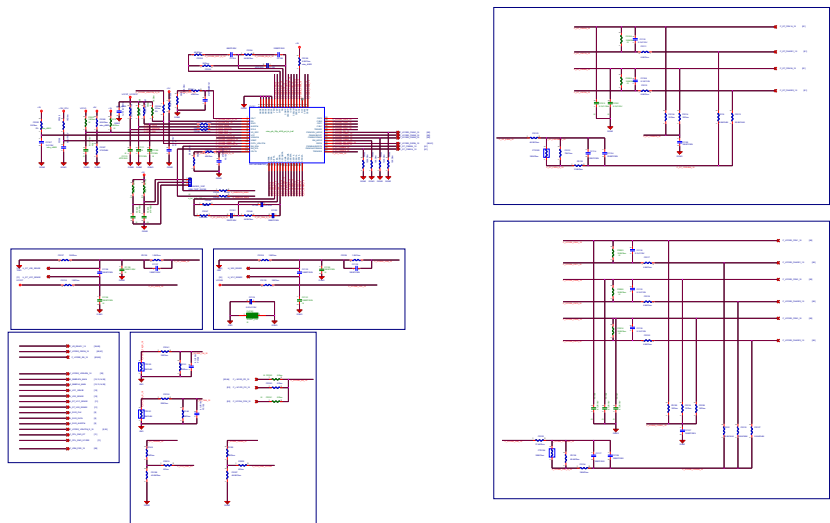
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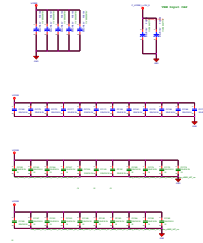
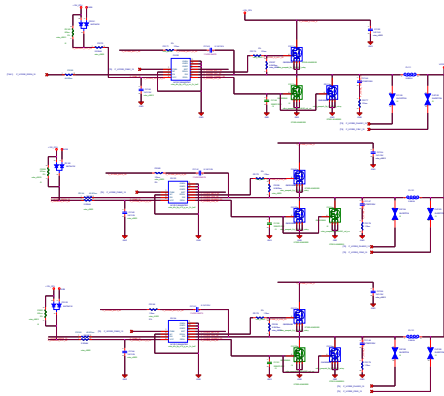


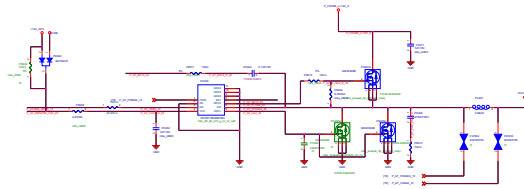
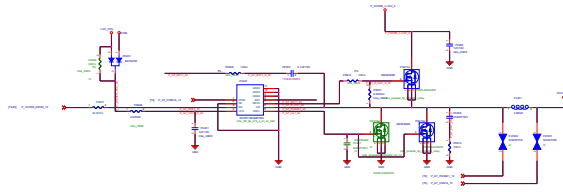
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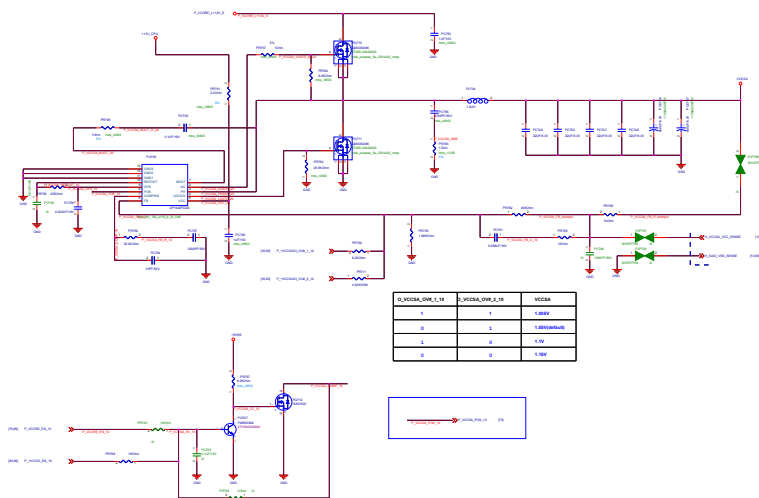
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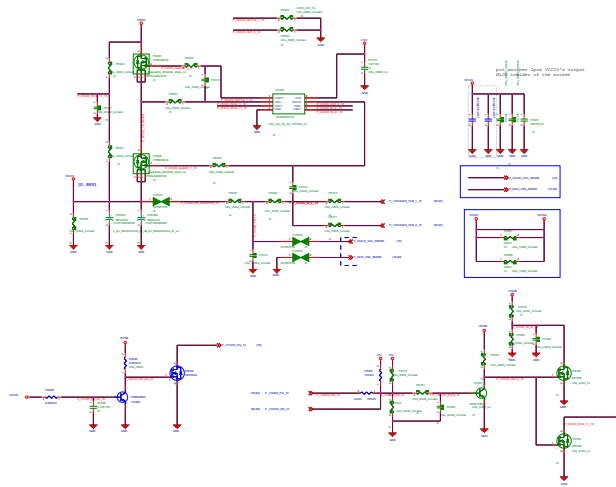


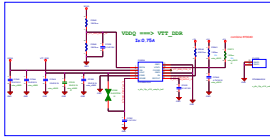
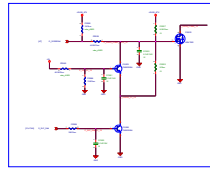
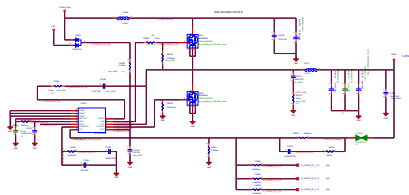




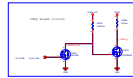
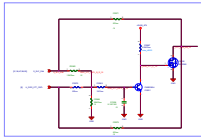
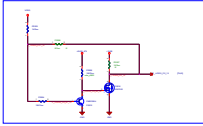


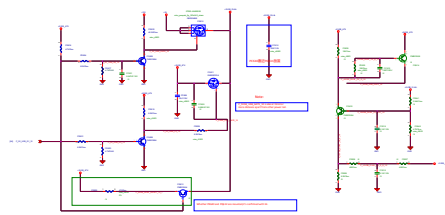


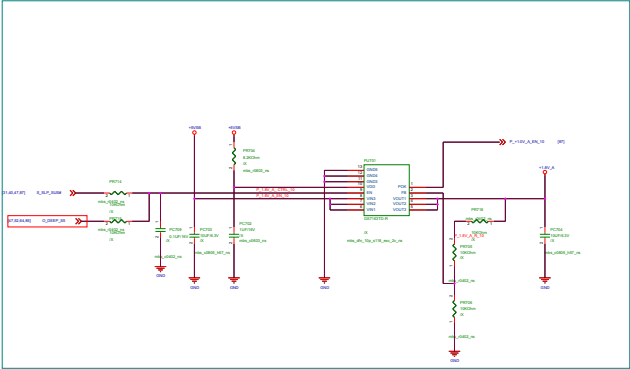
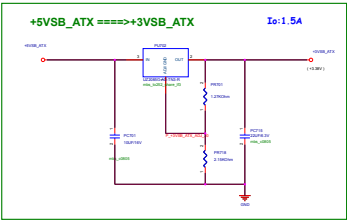


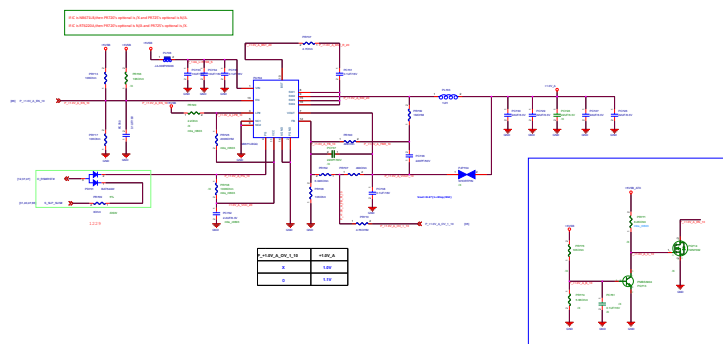


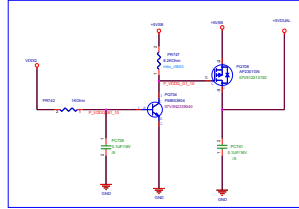
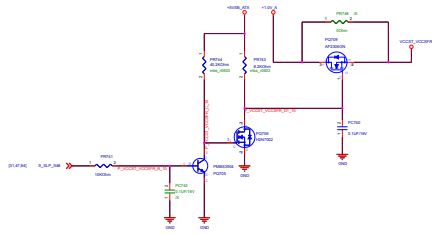
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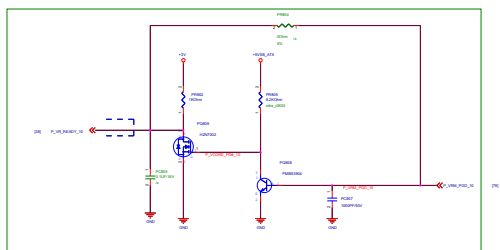
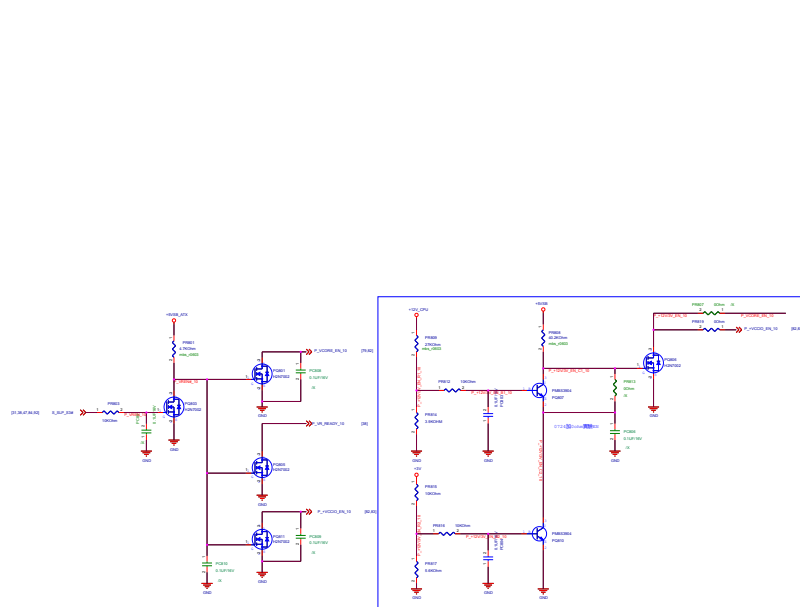


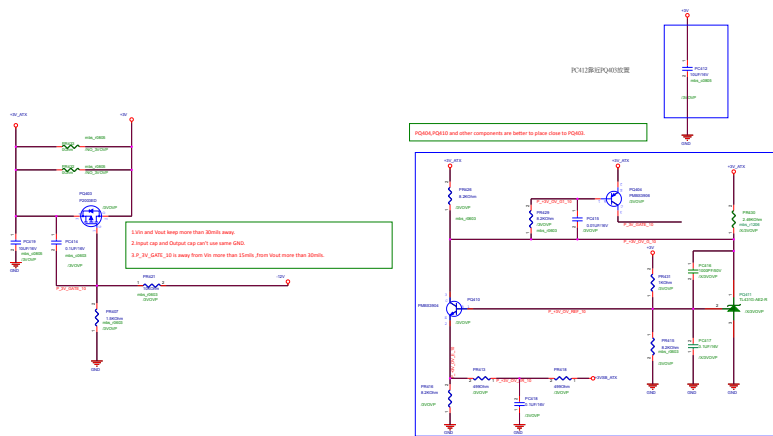


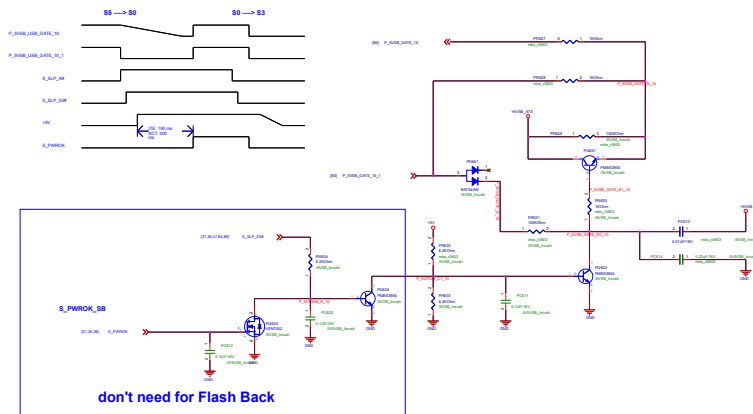












Inrush Circuit for USB Port default have Power or Flash Back Function

